Frequency Multipliers
Design Techniques and Applications

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• Introduction – applications
• Noise Concepts in Frequency Multipliers
• Harmonic generation – classical method
• Broadband multipliers
• Advanced concepts in odd-order multiplier design
• Conclusion
Terahertz Receiver for Radio Astronomy

Introduction
Introduction

Terahertz Receiver – cont’d

750 GHz diode multiplier

Introduction

Communications Receiver Front-End

- LNA
- Bandpass Filter
- Mixer
- Lowpass Filter
- IF Amp
- Demodulation Circuitry

Local Oscillator

Microwave Front End

Digital Back End

- XTAL oscillator
- SRD multiplier
- Bandpass Filter
- Amp
- MMIC multiplier
- Bandpass Filter
Noise Concepts

An oscillator’s output has amplitude and phase fluctuations

\[ u(t) = A(t) \cos[\omega(t)t] = A(t) \cos \left[ \omega_0 t + \frac{d\phi(t)}{dt} t \right] \]

The noise spectral density of the signal is

\[ S_\phi(f_m) = 10 \log \Delta \phi_{rms}^2 = 20 \log \Delta \phi_{rms} \]

After frequency multiplication we obtain

\[ v(t) = B_0 \cos \left[ n\omega_0 t + n\Delta \phi(t) \right] \]

\[ S_\phi^{(n)}(f_m) = 20 \log (n\Delta \phi_{rms}) = 20 \log n + 20 \log \Delta \phi_{rms} \]

phase noise degradation relative to input signal
Why frequency multiplication is “worth it”

• Typical phase noise (PN) of a 10 MHz Crystal Oscillator:

  \[-170 \text{ dBc/Hz } @ 100 \text{ kHz offset}\]

• Using a multiplier chain to get a 2.4 GHz signal degrades this phase noise by 20\log(240) = 48 \text{ dB}, yielding:

  \[-170 \text{ dBc/Hz } + 48 \text{ dB } = -122 \text{ dBc/Hz}\]

• Compare this to an on-chip LC-tank oscillator at 2.4 GHz which has a typical PN of \[-100 \text{ dBc/Hz } @ 100 \text{ kHz offset}\]
Multiplier Techniques

Classic FET multiplier topology [6]

\[ i_{ds} = I_{DS} + \sum_{n} I_n e^{j\omega n t} \]

where:

\[ I_n = I_{pk} \frac{4t_0}{\pi T} \left| \frac{\cos(n\pi t_0/T)}{1 - (2nt_0/T)^2} \right| \]
Harmonic Generation using a FET

Multiplier Techniques
Distributed Multipliers

Broadband Multiplier Designs

A. M. Pavio et. al., “A Distributed Broadband Monolithic Frequency Multiplier,”
Distributed Multipliers

Broadband Multiplier Designs

New Concepts in Tripler Design

Typical approach:
clip a sinusoid to generate lots of harmonics and then filter what is not needed

Wave-shaping technique:
make “deep cuts” in the wave to enhance the third harmonic only
Frequency Tripler

Tripler Circuit Implementation

Frequency Tripler

Circuit Core

![Circuit Diagram]

(a) Voltage waveform with TH₁ and TH₄
(b) Voltage waveform with TH₂ and TH₃
(c) Current waveform with and without cuts

Input Stage
Nonlinear Combiner
Frequency Tripler

Measured Results

Conversion Loss = 9.5 dB
Phase Noise Degrad. = 9.75 dB
Theoretical minimum is 9.54 dB
Fundamental Rejection > 11 dB
2\textsuperscript{nd} Harmonic Rejection > 9 dB
4\textsuperscript{th} Harmonic Rejection > 20 dB
Mixers with LO multiplication

Active x2 Subharmonic Mixer (SHM)

Standard Gilbert Cell

x2 LO multiplication
Mixers with LO multiplication

**x2 SHM Operation Details**

\[ v_{LO0} = A_{LO} \sin(\omega_{LO} t) \]

\[ i_1 = i_a + i_b = \mu_n C_{ox} \frac{W_1}{L} (V_{GS(LO)} - V_t)^2 + \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L} (v_{LO0}^2 + v_{LO180}^2) \]

\[ i_1 = \mu_n C_{ox} \frac{W_1}{L} (V_{GS(LO)} - V_t)^2 + \mu_n C_{ox} \frac{W_1}{L} v_{LO0}^2 \]

Using the relationship, \[ v_{LO0}^2 = v_{LO180}^2 \]
Frequency Multiplication using SHM’s

**Recent Advances**

**Frequency Tripler with Fundamental Signal Cancellation**

*No output filtering needed*

Recent Advances

Frequency Tripler Design

The feedforward path: Phase Shifter & Amplifier

x2 Subharmonic Mixer
Recent Advances

Frequency Tripler Design – cont’d

From the SHP Mixer

Balun

$V_{DD}$

$R_b$

$V_{SHM0}$

$V_{SHM}$

$V_{SHM180}$

From the feed-forward circuit

Subtractor

$V_{DD}$

$R_i$

$i_{SHM}$

$i_g$

$V_{Sub}$

$V_{Si}$

$V_{S2}$

Output buffer

$V_{DD}$

$R_L$

$V_{OUT}$
Recent Advances

Measured output spectrum

Input Freq. \( 1 \ \text{GHz} \)
Input power \(-10 \ \text{dBm}\)
Output Freq. \( 3 \ \text{GHz} \)
Conv. Gain \( 3 \ \text{dB} \)
Fund. Reject. \( 30 \ \text{dB} \)
Recent Advances

Measured power performance

High suppression of the fundamental and other harmonics achieved without on-chip or off-chip filtering.
Recent Advances

PN Degradation Performance

Phase noise degradation: 9.69 dB

Theoretical minimum: $20 \log(3) = 9.54 \ dB$
Conclusion

- Local Oscillator signal generation is a key driving force behind frequency multiplier design.
- Multiplying a very stable low-frequency reference signal can still produce signals with better phase noise than producing them on-chip in the microwave range.
- Wave-shaping techniques can be exploited to generate odd-order multipliers.
- Recent advances in multiplier design have led to highly compact circuits with excellent fundamental rejection that do not require output filtering.
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References


2. A. M. Pavio et. al., “A Distributed Broadband Monolithic Frequency Multiplier,” 


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