Active quasi-circulator with high port-to-port isolation and small area

S. He, N. Akel and C.E. Saavedra

An active quasi-circulator integrated circuit relying on a differential central core is presented. Measurements on the quasi-circulator reveal that the forward transmission coefficients, $S_{12}$ and $S_{23}$, are both close to -4 dB in the range of 2.5 to 6 GHz. The isolation between the ports is greater than 20 dB and can reach up to 59 dB in the case of $S_{21}$. The chip was fabricated on a standard 130 nm CMOS process and the core circuit area measures 0.105 mm$^2$, making it the smallest active quasi-circulator known to date.

Introduction: A considerable number of active quasi-circulator circuits have been demonstrated to date in both hybrid and RFIC form [1–6]. A key reason to use an active quasi-circulator compared to a passive ferrite-based one is to reduce cost. Hybrid and RFIC implementations have their own respective advantages in relation to cost and which circuit is selected is dependent on the end-use of the quasi-circulator. For medium-power applications, for example, a hybrid circuit might be a better solution than an RFIC implementation because relatively inexpensive packaged power transistors can be easily found. Of course, one drawback of the hybrid circuit is its large area. For small-signal applications, a general-purpose RFIC quasi-circulator can be the more cost-effective choice. In this Letter, we report a quasi-circulator CMOS RFIC that relies on a novel differential circuit topology. A pair of transconductor circuits are used to convert differential voltage signals to current signals which can be summed to provide isolation between two of the ports. This quasi-circulator has the smallest active area known to date, measuring only 0.105 mm$^2$.

Quasi-circulator circuit: A schematic diagram of the proposed quasi-circulator is shown in Fig. 1. First, note that the circuit accepts a differential signal at port 1 while ports 2 and 3 are single-ended. The in-phase component at port 1 passes through a common-gate NMOS device, $M_1$, and exits at port 2. When a signal is incident at port 2 the signal will travel in the forward direction through the top transconductor circuit ($g_{m1}$) and exit at port 3.

Although the buffer increases the DC power consumption of the chip, it is capable of providing a reasonably low reflection coefficient over a wide frequency band and, furthermore, it takes up a very small amount of area compared to the alternative of using a tuned, passive, matching network.

Experimental results: To demonstrate the quasi-circulator concept, a chip was fabricated using a standard 130 nm CMOS process from IBM. Small-signal, large-signal and noise figure measurements were carried out directly on-wafer.

The input impedance to the transconductance stage in Fig. 2 is high and therefore some type of matching circuit is necessary to avoid a high reflection coefficient at port 2. The solution chosen in this design was to insert a buffer stage with a moderately low input impedance ahead of the transconductance stage. The buffer is a simple common-source amplifier with resistive feedback. Although the buffer increases the DC power consumption of the chip, it is capable of providing a reasonably low reflection coefficient over a wide frequency band and, furthermore, it takes up a very small amount of area compared to the alternative of using a tuned, passive, matching network.

The measured port-to-port isolations are shown in Fig. 5. The port 1 to port 3 isolation, $S_{21}$, is typically the most challenging to reduce in the active quasi-circulator design because it is in the forward path of the signal flow. In this chip, the $S_{21}$ isolation is obtained through signal cancellation and it is between 20 and 21 dB, a result that compares well with other quasi-circulators reported in the literature (see Table 1). The port 2 to port 1 isolation, $S_{31}$, was between 23.4 and 24.5 dB, while the port 3 to isolation, $S_{23}$, was between 30.6 and 40.3 dB. The best isolation, as expected, was from port 3 to port 1 ($S_{31}$) with a value between 42.7 and 59 dB over the measured frequency band.

RF power measurements were carried out at 6 GHz. With the incident signal applied at port 1 and the output taken at port 2, the IP$_{1dB}$ was measured at $+3$ dBm. In addition, a two-tone test was done with the centre frequency at 6 GHz and a tone spacing of 1 MHz. The two-tone revealed an IP$_{2}$ from port 1 to port 2 of $+16.9$ dBm. Lastly, noise figure (NF) measurements were also conducted and the average NF from port 1 to port 2 was 14 dB while for port 2 to 3 it was between 6 and 8 dB over the frequency span of 2.5 to 6 GHz.

Fig. 1 CMOS quasi-circulator schematic diagram

Fig. 2 Transconductance stage
Conclusion: A new active quasi-circulator has been demonstrated in which the forward isolation between ports 1 and 3 is obtained through the use of signal cancellation. The cancellation is realised by converting the differential voltage signal at port 1 to current signals and then adding them together at the output node. The chip exhibits excellent isolation between all of the ports and the forward insertion loss from ports 1 to 2 and from ports 2 to 3 has good flatness.

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One or more of the Figures in this Letter are available in colour online.
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References

Table 1: Summary and comparison table

<table>
<thead>
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<th>Frequency (GHz)</th>
<th>This work</th>
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<th>[4]</th>
<th>[5]</th>
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<td>2.5–6</td>
<td>29–31</td>
<td>1.5–2.7</td>
<td>1.5–9.6</td>
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<tr>
<td>Size (mm²)</td>
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<td>0.25</td>
<td>0.41</td>
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<td>IP_{1dB} (dBm)</td>
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<td>–7</td>
<td>–6.4</td>
<td>–3.7</td>
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<td>Power (mW)</td>
<td>66</td>
<td>15</td>
<td>86</td>
<td>31.6</td>
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<td>S_{21} (dB)</td>
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<td>–4 to –6</td>
<td>2.4 to 1.5</td>
<td>–5 ± 1</td>
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<tr>
<td>S_{32} (dB)</td>
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<td>–7.2 to –7.9</td>
<td>0 to –3</td>
<td>–5 ± 1</td>
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<td>S_{11} (dB)</td>
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<td>&gt;12</td>
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<td>&gt;18</td>
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<td>S_{12} (dB)</td>
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<td>&gt;30</td>
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<td>S_{23} (dB)</td>
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<td>&gt;17</td>
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