Latch-up: Causes and Prevention

ELEC 353 – Electronics II

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What is Latch-up?

It is the activation of parasitic bipolar devices in a CMOS integrated circuit. The result is a **low-impedance path** from the chip power supply to ground.
Background

• The parasitic bipolar devices in a CMOS chip create a device known as a Thyristor.

• Thyristors are also known as silicon-controlled rectifiers (SCR’s).

• These devices have 4 alternating n and p layers.
A thyristor is a normally OFF device with minimal current flow.

Current will flow from node A to K when a control signal is applied at node G.

When triggered into the conducting state, the thyristor is said to be latched.
Thyristor operation

Step-by-step:

1. Current is injected into the base of Q2 (the “gate”).
2. This is followed by current flow in the BEJ of Q1.
3. Q1 turns fully ON causing more current to flow into the base of Q2.
4. Which causes more current flow in Q1, creating a positive feedback loop.
Thyristor operation

• When the thyristor is latched, the control signal does not have any effect.

• Therefore, there is an uninterrupted low-impedance path from the positive to the negative supply, or ground pin.

• The trigger signal can be a voltage surge, or spike, of sufficiently long duration.
Thyristor operation

- The thyristor can be shut off if the current flow drops below the holding value, $I_H$.

- Another way to shut off the thyristor is to turn off the power supply.
Parasitic Thyristors in CMOS

CMOS inverter

Basic model

Figures from Redmond
Parasitic Thyristors in CMOS

A more detailed model

Figures from Haseloff
Parasitic Thyristors in CMOS

• When latch-up occurs, a large current flows in the CMOS circuit, leading to overheating and eventual failure.

• The individual bipolar devices have low current gain, with a $\beta < 1$. Therefore, large current spikes are needed to activate them.

• The cutoff frequency of the transistors is low because of the large device dimensions: $f_T \approx 1$ MHz.
Parasitic Thyristors in CMOS

• Therefore, very short duration pulses cannot trigger the thyristor because the devices are not fast enough to respond.

• However, with device scaling the parasitic thyristor’s frequency response also improves, meaning it becomes more sensitive to short duration pulses.
Latch-up triggering mechanisms

- An input or output voltage that is higher than the supply voltage, $V_{DD}$.

- An electrostatic discharge (ESD) event can trigger a thyristor due to the high voltages and currents involved.
Latch-up triggering mechanisms

• While an ESD event has a very short duration, the chip is flooded with charge carriers, which flow away slowly, resulting in the triggering of the thyristor.

• Caused by ionizing radiation found in:
  – The upper atmosphere or outer space
  – High energy sources in a lab environment
  – Nuclear power plants
Latch-up prevention

- Stay below the absolute maximum ratings of the chip.
- Isolate the NMOS and PMOS devices using an oxide trench together with a buried oxide layer:

![Diagram of Latch-up prevention](Figure from Redmond)
Latch-up prevention

- If you cannot include an oxide trench, then use guard rings around your devices:

Figure from Haseloff
Latch-up prevention

The idea behind using a guard ring is:

to add more collector terminals to the parasitic transistors in order to steer the current flow away from the desired devices.
Latch-up protection

- Use reverse biased diodes between the input/output pins and the voltage supplies.
- Schottky diodes are preferred because of their low forward resistance.

Figure from Microchip AN763
Latch-up prevention

• Improper grounding can cause latch-up.

• The PWM source outputs a low signal to the inverter, which turns on the MOSFET.

• If the parasitic trace resistance (R1) is large enough, the ground of the inverter can be at a higher potential than the input signal which will cause latch-up.

Figure from Microchip AN763
Latch-up prevention

• Using proper grounding can avoid latch-up by using common ground point connections.

• Using a common ground line is not effective because the parasitic resistance in the ground line is defeats the purpose.
Review

• Latch-up can be triggered by voltage spikes applied to the input of a chip.

• The spikes have to be larger than the supply voltages of the chip.

• ESD events can trigger latch-up because of the large current flows involved.