

A Compact Tunable 5GHz-Band Quadrature Downconverter with an Integrated 90° Phase Shifter and Balun

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Abstract

In this paper, a compact tunable quadrature downconverter is demonstrated using double-balanced Gilbert-cell mixers with the RF transconductor shared between them to reduce mismatches and improve the output I-Q balance. An RC polyphase network is used to generate the quadrature LO signals, which employs variable NMOS resistors for fine-tuning after fabrication. The integrated circuit (IC) is experimentally demonstrated showing good performance in the 5GHz band, with the conversion gain exceeding 3dB and the I-Q imbalance being less than 4° and 0.6dB. The IC occupies an active area of only 650µm by 620µm and consumes less than 23mW from 1.6V.

1. Introduction

Quadrature downconversion using 90° out-of-phase carriers is frequently employed in radio frequency (RF) phase shift-keying demodulators and direct-conversion or low intermediate frequency (IF) receivers [1]. It is commonly achieved by having two separate mixers in parallel driven by quadrature local oscillator (LO) signals [1, 2]. This approach significantly augments integrated circuit (IC) size, cost and power consumption. In addition, process variations introduce mismatches between the two mixers, creating a phase and amplitude imbalance between the generated in-phase (I) and quadrature-phase (Q) IF signals thus degrading performance [1]. Furthermore, widely used methods to generate the quadrature LO signals, such as frequency divide-by-two circuits (DTCs) [2, 3] and resistor-capacitor (RC) networks [4], can be impractical and particularly sensitive to device mismatches at high frequencies, which lead to additional phase and amplitude errors. They can also consume a considerable amount of DC power or occupy significant IC space.

In this paper, a quadrature downconverting mixer is demonstrated based on the double-balanced Gilbert-cell, which provides good conversion gain and port-to-port isolation. The input RF transconductor is shared between the two quadrature LO switching cores to reduce mismatches and improve the I-Q balance [3, 5]. Such sharing also saves IC space, as only one differential pair and its associated biasing network is needed. An RC polyphase network [6] is used to generate quadrature LO signals, with variable NMOS resistors employed for fine-tuning to minimize phase errors after fabrication. This also allows for LO frequency tuning of the downconverter. The RF signal is split on-chip into two differential signals using a compact common-gate, common-source (CG-CS) balun [4]. The circuit is experimentally demonstrated in 0.18µm CMOS showing good performance in the 5GHz band, with the conversion gain exceeding 3dB. An accurate I-Q balance is also achieved, with the phase and amplitude errors being less than 3.6° and 0.58dB. The IC measures 750µm by 750µm with an active area of only 650µm by 620µm, and consumes less than 23mW from a 1.6V supply.

2. Circuit Architecture and Design

A circuit schematic of the quadrature mixer is shown in Fig. 1. It consists of a double-balanced Gilbert cell with the input transconductor pair M1-M2 shared between the quadrature mixing cores M3-M6 and M7-M10 [3]. This eliminates the mismatch between the I-Q outputs due to the RF transconductance and saves IC space. Since the LO differential pairs M3-M6 and M7-M10 are overdriven to behave like alternating switches, their mismatch is comparatively negligible [5].

Since the mixer (Fig 1) has two stacked levels of transistors, its use with a low supply voltage (1.8V in 0.18µm CMOS) entails a significant tradeoff between linearity and gain. This can be seen by writing a first-order expression for the voltage conversion gain (A_v) as [7]:

$$A_v = g_m R_L = \frac{2I_D}{V_{GS} - V_T} \frac{V_{RL}}{I_D} = \frac{2V_{RL}}{V_{GS} - V_T} \quad (1)$$

where g_m is the transconductance of M1-M2, R_L is the output load resistance, I_D is the bias current, $V_{GS}-V_T$ is the gate-source overdrive voltage of M1-M2, and V_{RL} is the voltage drop across the load resistors R_L . It is clear that there is a tradeoff between gain (A_v) and linearity ($V_{GS}-V_T$) for limited supply headroom (V_{RL}). However, the bias current and power can be reduced while keeping the same gain and linearity by decreasing the transistor widths to keep their gate overdrive ($V_{GS}-V_T$) intact and increasing the load resistance to restore the gain [8].

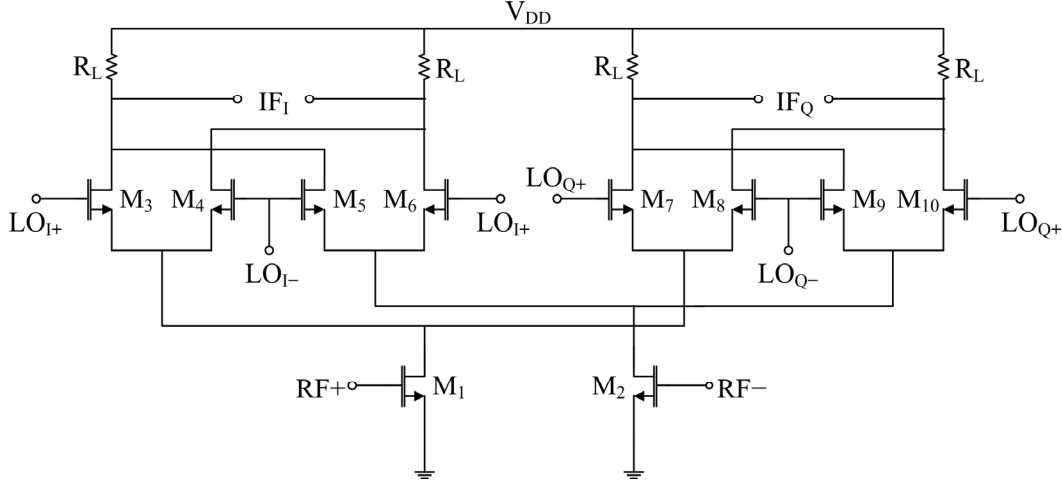


Fig. 1: Circuit schematic of quadrature downconverter.

As shown in Fig. 1, the source of the transconductor pair (M1, M2) is grounded as opposed to being connected to a tail current source. This increases their gate-source overdrive and reduces third-order coupling for higher linearity [9]. It also relaxes the voltage headroom, allowing further improvements in gain and linearity. Ultimately, the widely used tail current mirror and source degeneration inductors are not necessary, saving significant IC space.

The accuracy of generating quadrature LO signals also affects the balance of the downconverted I and Q signals at the output. Several techniques have been developed to generate 90° phase shifters with low phase and amplitude errors [2-4]. A single-stage tunable RC polyphase network is used here for its small area and zero DC power consumption. It also has less signal loss compared to using two RC-CR circuits, as it combines the two balanced signals as opposed to splitting each signal separately. Fig. 2 shows the polyphase network and how it operates [6]. It generally has an all-pass response (unity gain) with the desired 90° phase difference appearing at the cut-off frequency of $1/(RC)$, where the differential inputs are shifted by $\pm 45^\circ$ towards each other before they are combined. Therefore for the relatively high 5GHz band, a small RC product is required allowing small resistors and capacitors to be used. However integrated polysilicon resistors can exhibit large tolerances (more than 20%) for small resistance values (below $1k\Omega$). Such high tolerances are critical, as discrepancies will change the cutoff frequency introducing phase errors at the frequency of interest. For this reason, a variable resistor in the form of an NMOS transistor biased in the triode region is used, with the resistance controlled by a tuning voltage V_{TUNE} applied to the gate (Fig. 2). Its effective resistance R is approximately given by:

$$R \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{TUNE} - V_T)}, \quad (2)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor, and V_T is the threshold voltage. It is clear that the resistance R is inversely proportional to the tuning voltage V_{TUNE} and can be varied to adjust the cut-off frequency after process variations for the lowest possible phase error. This ultimately enables LO frequency tuning of the quadrature downconverter.

The input RF signal is split on-chip into two differential signals using an active CG-CS balun that drives the transconductor pair M1-M2 (Fig. 1) [4]. An active balun is advantageous for its compact area and ease of IC

integration as opposed to a passive structure, which could be prohibitively large in this frequency range. It also exhibits a more wideband performance with a low input reflection coefficient and a good phase and amplitude match [4].

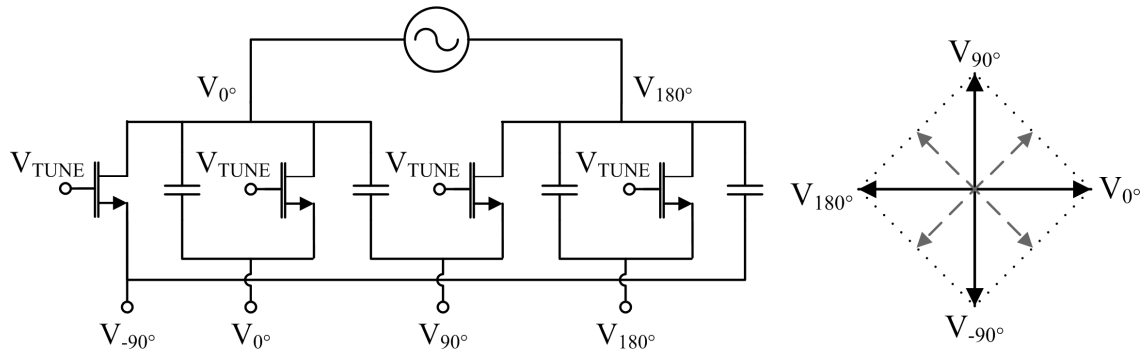


Fig. 2: RC polyphase network schematic and operation.

3. Experimental Results

The quadrature downconverter was fabricated in a standard $0.18\mu\text{m}$ CMOS process. A photograph of the IC is shown in Fig. 3. It occupies a total die area of $750 \times 750 \mu\text{m}^2$ including bonding pads and the active circuit area is only $650 \times 620 \mu\text{m}^2$. The circuit consumes less than 14mA of current from a 1.6V voltage supply.

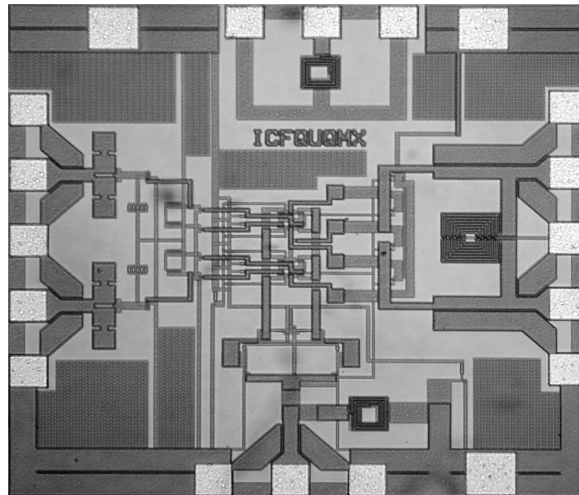


Fig. 3: Photograph of the quadrature downconverter IC.

A direct on-wafer measurement of the IC was carried out using co-planar RF probes and DC probes. The RF and LO signal power levels were set to -20dBm and -4dBm , at frequencies of 5.5GHz and 5.25GHz respectively. The tuning voltage V_{TUNE} was also set to 1.2V , as this was found to give the best I-Q balance at the output. Fig. 4(a) shows the output spectrum with the 250MHz IF having a power level of about -16.4dB for a conversion gain of 3.6dB . The output I and Q signals were also measured in time-domain using a digital sampling oscilloscope and a screenshot is shown in Fig. 4(b). The phase deviation from quadrature is approximately 3.6° and the amplitude mismatch is about 0.58dB . It should be noted that all of these measurements were made without filtering the outputs of the IC. Table 1 summarizes the measured performance including the input RF 1dB compression point ($P_{1\text{dB}}$) and return loss.

4. Conclusion

A compact tunable quadrature downconverter has been developed in $0.18\mu\text{m}$ CMOS using Gilbert-cell mixers with the RF transistor shared between them to reduce mismatches and improve the I-Q balance. A

single-stage variable RC polyphase network is used to generate quadrature LO signals, which allows for fine-tuning after fabrication to trim the output phase and amplitude errors.

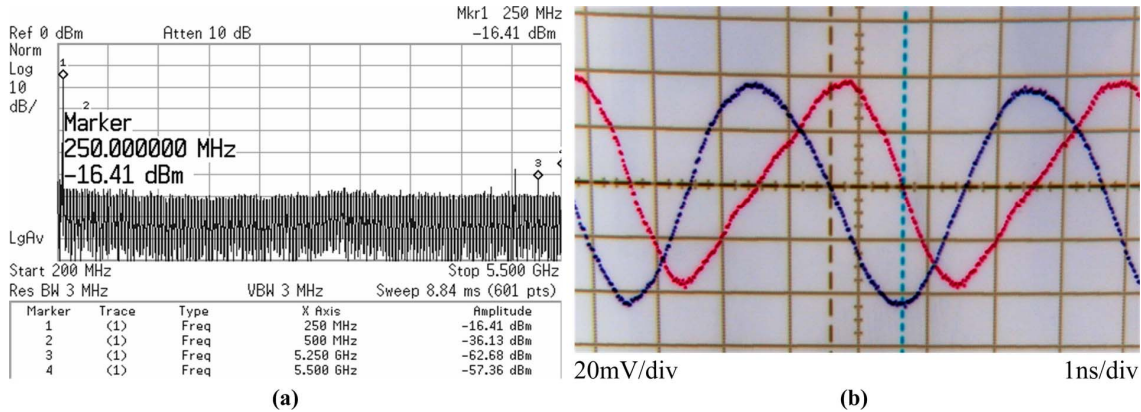


Fig. 4: (a) Downconverter output spectrum and (b) I and Q time-domain waveforms.

Table 1: Summary of quadrature downconverter characteristics.

CMOS Technology	Area	DC Power	RF Input Match	Gain	RF Input P_{1dB}	I/Q Mismatch
0.18 μ m	650 \times 620 μ m ²	23mW at 1.6V	-12dB	3.6dB	-12dBm	3.6°, 0.58dB

5. References

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