

A COMPACT CAPACITOR COMPENSATED WIDEBAND BALUN IN CMOS TECHNOLOGY

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ABSTRACT

A novel balun manufactured in standard CMOS 0.18 μm is proposed that demonstrates a very large wideband operation. This device achieves this through the use of an external compensating capacitor to counter the effects of parasitic capacitances. An input stage common gate amplifier is then used to improve the return loss and provide additional gain. The fabricated active balun using the proposed circuit shows that the device performs with a 7.5 GHz bandwidth centered at 3.5 GHz. In addition an excellent 15 dB return loss, -5.8 dBm compression point and 12 mW power consumption are also reported.

1. INTRODUCTION

The basic concept of a balun is to convert an unbalanced signal into a balanced one. This is of particular importance in many transceiver designs where there is a need for a balanced system. For example many receivers use a monopole antenna which produces an unbalanced signal. In order to use a balanced mixer (such as a gilbert cell) a balun is required to convert the signal.

In general baluns are placed in two categories: Active and passive. Active baluns are advantageous because they have lower loss and are significantly smaller to implement onto an monolithic microwave integrated Circuit (MMIC) design. However their designs can often be very complicated and are prone to a much smaller bandwidth. Passive baluns such as the Marchand do not consume any power and have a larger bandwidth (up to 100%), however suffer from their large size especially at the RF frequencies [1] [2].

In the trend to produce system on chip (SoC) solutions, the use of low resistivity silicon produces passive components that are excessively lossy. Thus for most MMIC designs, passive elements such as coplanar waveguides (CPW) and inductors are avoided. Therefore active baluns provide a good solution given the acceptable loss in bandwidth. In this paper we present a single transistor balun and investigate its parasitics that cause the limited bandwidth both through theory and simulation. The design is then improved upon by

This work was supported by the Natural Sciences and Engineering Research Council (NSERC)

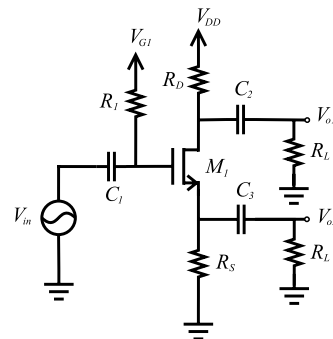


Fig. 1. Single Transistor Balun Schematic

inserting a compensating capacitor to significantly increase its operational bandwidth and allow this active balun to potentially replace passive baluns at the lower microwave frequencies where the size is very critical.

2. CIRCUIT DESCRIPTION

2.1. Single Transistor Balun

A common type of balun is a single transistor balun shown in Figure 1. The input signal is applied to the gate (v_{in}) and the output is taken from both the drain (v_{o1}) and the source (v_{o2}). The circuit can be viewed as a typical common source (CS) amplifier if the output at the source is ignored and as a common drain (CD) amplifier if the source output is ignored. The transfer function for a CS amplifier has a 180° phase offset relative to the input, while the transfer function of a CD has a 0° phase offset relative to the input. The resulting output of phase output signals are correspondingly 180° from each other, thus producing a balanced signal from an unbalanced one.

2.2. Miller Capacitance

Because of the capacitance from the gate to drain C_{gd} , it is difficult to analyze the circuit, as such Miller's theorem describes a way in which the capacitance across the input to the output of an amplifier can be separated in order to aid in the analysis. Typically, the Miller theorem is used to describe

the parasitic effects of C_{gd} where at high frequencies the gain rolls off.

After applying the Miller transformation, the impedance from gate to source Z_{gs} and gate to drain Z_{gd} can be shown to be (1) and (2).

$$Z_{gs} = \frac{-j}{\omega(C_{gs} + C_{gd}(1 - K))} \quad (1)$$

$$Z_{ds} = \frac{-j}{\omega(C_{gd}(1 - \frac{1}{K}))} \quad (2)$$

(3)

Where R'_S , R'_D and K are as follows:

$$R'_S = R_S \parallel R_L = \frac{R_S R_L}{R_S + R_L} \quad (4)$$

$$R'_D = R_D \parallel R_L = \frac{R_D R_L}{R_D + R_L} \quad (5)$$

$$K = \frac{V_{o1}}{V_{in}} = \frac{-g_m R'_D}{1 + g_m R'_S} \quad (6)$$

Circuit analysis is then performed using (1), (2), (3), (5) and (6) in order to determine the gain at each output shown in (7) and (8).

$$\frac{v_{o2}}{v_{in}} = \frac{Z_{ds}^2 + R'_D Z_{ds} + g_m Z_{gs} Z_{ds}^2 + \dots}{R'_S Z_{ds} Z_{gs} + R'_S Z_{ds}^2 + R'_D R'_S Z_{ds} + \dots} \quad (7)$$

$$\frac{g_m R'_D Z_{gs} Z_{ds} - g_m R'_D Z_{gs} Z_{ds}}{g_m R'_S Z_{gs} Z_{ds}^2 + Z_{gs} Z_{ds}^2 + R'_D Z_{gs} Z_{ds}}$$

$$\frac{v_{o1}}{v_{in}} = \frac{V_{o2} R'_D - g_m R'_D Z_{ds} + g_m R'_D Z_{ds} v_{o2}}{Z_{ds} + R'_D} \quad (8)$$

The transfer functions are then plotted in Matlab and are shown as a dashed line in Figure 2. The amplitude balance is defined as the ratio of the two output powers in decibels and the phase balance is defined as the difference in phase in degrees. Ideally the phase balance should be at 180° and the amplitude balance at 0 dB. Although the Miller effect produces shunting effect with regards to the gain at high frequencies, its effects as seen in simulations are of more concern with regards to the phase. It is acceptable for the total gain of the system to roll off in a balun design, however mismatch in both the phase and amplitudes is of primary concern.

2.3. Compensating Capacitor

From the Matlab results, it is clear that the one-transistor active balun has very limited phase balance over frequency (i.e. bandwidth). For this reason in order to increase the bandwidth a solution must be found to force the phase to 180° . A reactive element placed somewhere in the circuit is sought that will move the phase back at higher frequencies, but also proportionally compensate less at lower frequencies.

In order to produce such a schematic, consider the circuit in Figure 3a): if a capacitor C_c is placed in parallel with a

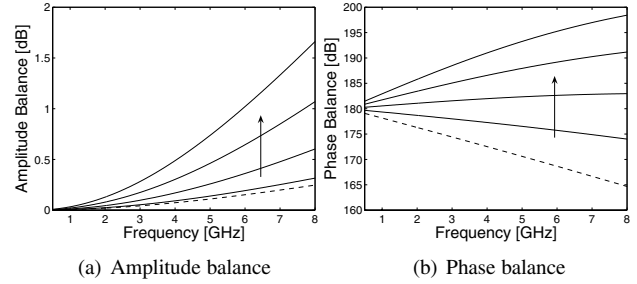
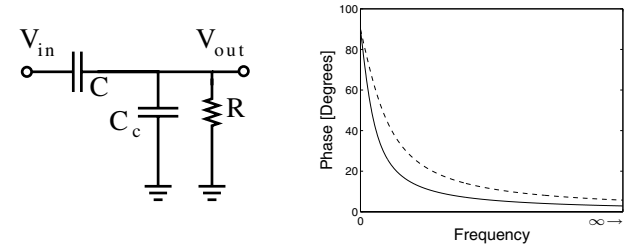


Fig. 2. Matlab results for analytical equations, the dashed line is the original balun and the solid lines are the various values of C_c swept from 100 to 400 fF



(a) Example circuit for compensating the phase (b) Phase plot where the solid line is with C_c and the dashed line is without

Fig. 3. Effects of C_c on a simple RC circuit

resistor R , the resulting plot of the phase with and without C_c is seen in Figure 3b). The solid line shows that for some value of C_c , the phase with respect to the input will be reduced compared to the original circuit without C_c . Note that at low frequencies, the amount of change due to C_c is very little, but the difference C_c makes in phase increases and then decreases again. If we now refer back to the circuit in Figure 3a) it is evident that it is similar to the capacitor and resistive network at the input/output of v_{o2} in the balun circuit.

The effectiveness of the compensating capacitor tapers off at very high frequencies. This is seen in Figure 3b) in which the transfer function with the compensating capacitor depicted as a dashed line is simulated. Because C_c overcompensates at mid frequencies and then undercompensates at high frequencies, any C_c has an upper limit to the bandwidth in terms of phase that can be compensated.

If the compensating capacitor is inserted to the original schematic as shown in Figure 4, all of the previously derived equations are still valid except for R'_S . The new R'_S is then shown to be (9).

$$R'_S = R_S \parallel R_L \parallel C_c = \frac{R_S R_L}{j\omega C_c R_S + j\omega C_c R_L + 1} \quad (9)$$

The derived transfer function was evaluated in Matlab with various compensating capacitances to determine their effects. Figure 2 demonstrates the effects of sweeping C_c from 100 to 400 fF. Additional device level simulations in Advanced Design Simulator (ADS) verified the results and were found

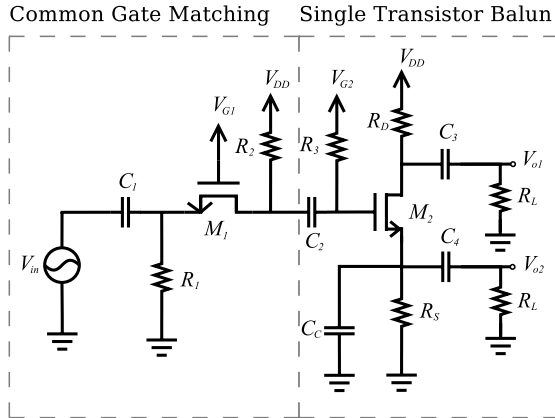


Fig. 4. Schematic of active balun including the common gate input stage

to be within 0.2 dB for the amplitude balance and 3° for the phase balance.

The arrow shows the trend as the capacitance is increased. It is seen that as C_c increases, the phase imbalance also increases. Because of the extra capacitance, the circuit begins to shunt more current at the source when compared to the drain, thus shifting the balance away from the original ≈ 0 dB amplitude balance. A compromise is chosen in the selection of C_c that gives a good phase balance and an acceptable amount of amplitude imbalance.

2.4. Common Gate Input Matching

The balun circuit used here has the input applied to the gate of the transistor. The input impedance looking into the gate is very high and behaves practically like an open circuit. Several methods exist to improve the input matching. However, it was elected to use a common gate (CG) amplifier to provide input matching because of its large bandwidth.

The schematic of the CG amplifier is shown in Figure 4. The input looking into the source of the transistor is approximately $1/g_m$. Because g_m is proportional to the width of the transistor, its size can easily scaled to match the input impedance of the 50 Ω system.

The resulting return loss proves to be a good match and gives an average of 20 dB return loss. In addition, the input referred 1 dB compression point (P_{1dB}) of 2 dBm and peak gain of 3.5 dB at 2 GHz were also reported. This shows good power handling and acceptable gain which enables us to operate this amplifier to very high power levels by CMOS standards in addition to offset the loss produced by the balun.

2.5. Final circuit

The final design with both the input matching common gate amplifier along with the one transistor balun is shown in Figure 4. The appropriate C_c was selected that gives the best phase and amplitude balance. The final layout was simulated

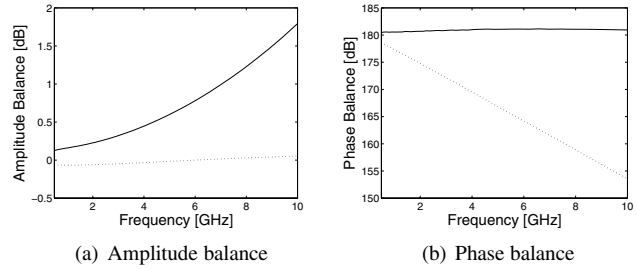


Fig. 5. Simulated parameters for final circuit where the dashed line is the original design and the solid line is the compensated balun

in SpectreRF. For reference, the design was simulated with and without the compensating capacitor. The original circuit demonstrates that the amplitude balance is closely matched past 8 GHz, however the phase balance decreases very rapidly. With the addition of the extra compensating capacitor C_c , the phase is kept to slightly above 180° and is shown as a solid line in Figure 5. However, the tradeoff here is that the amplitude imbalance has increased. Overall the circuit provides good amplitude and phase balance past 8 GHz. In addition, the device provides a peak unity gain and relatively low input reflection of 20 dB.

The final P_{1dB} is determined to be -5 dBm. The compression point is reduced because of the balun, however overall the performance is still acceptable and is still considered good power handling.

3. MEASUREMENT RESULTS

The device was connected to the test equipment using a CPW ground signal ground (GSG) probe for the input and a ground signal ground signal ground probe (GSGSG) for the outputs. The vector network analyzer set to an output power of -10 dBm and used to measure the phase and amplitudes of the outputs.

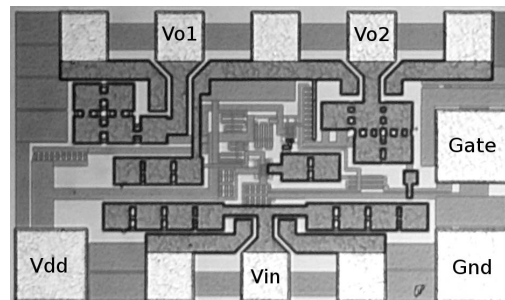


Fig. 6. Micro-photograph of active balun

Figure 8a) shows the amplitude and phase balance for the chip. The amplitude balance does not increase more than ± 1 dB over the frequency range between 500 MHz to 8 GHz. The phase balance begins just below 180° but increases to a

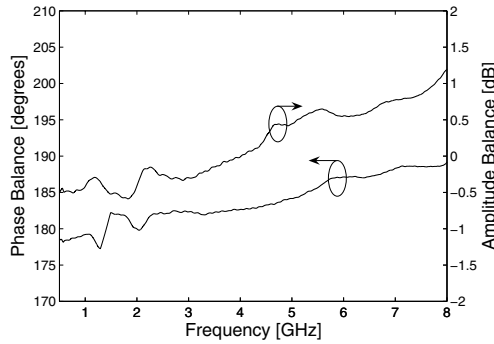


Fig. 7. Measured phase and amplitude balance

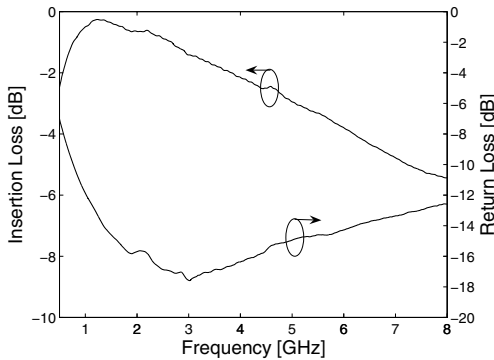


Fig. 8. Measured insertion loss and return loss

maximum of 190° over the same frequency range. The transmission loss of the device starts at 0 dB but rapidly declines to about -7 dB. It is concluded that this device performs exceptionally well across over a 7.5 GHz bandwidth.

For the input referred P_{1dB} compression point, the signal generator was swept and a spectrum analyzer used to determine the output power. The input referred P_{1dB} was measured at 2 GHz and it is found to be -5.8 dBm. A micrograph of the device is seen in Figure 6. The total size of the device was 300x510 μm or 0.153 mm² and 160x425 μm or 0.068 mm² without the DC and RF bonding pads.

$$FOM = \frac{\Delta f}{\Delta\phi\Delta A} \quad (10)$$

It is difficult to compare this work to existing literature on active baluns because each circuit defines its own acceptable phase and amplitude metrics. Thus a figure of merit (FOM) was devised in order to compare the baluns. The FOM formula used is found in (10). The data used and the resulting FOM is shown in Table 1. The devised FOM shows that this device outperforms the existing literature using CMOS processes by almost a factor of two.

This balun is able to perform with excellent phase and amplitude performance while maintaining very low power consumption and device area. In addition, its power handling capabilities as shown in the P_{1dB} compression point are the

	Δf	$\Delta\phi$	ΔA	FOM [GHz/° dB]
This work	7.5 GHz	8°	1.5 dB	0.625
[3]	1 GHz	4°	0.8 dB	0.313
[4]	3.5 GHz	5°	2 dB	0.350
[5]	10 GHz	8°	4 dB	0.313

Table 1. Values used to calculate figures of merit

	Freq. Band	S_{21}	S_{11}	P_{1dB}	Size	Power	FOM	Tech.
TW	0.5 – 8 GHz	-3 dB	-15 dB	-5.8 dBm	0.153 mm ²	12 mW	0.625	0.18 μm
[3]	5 – 6 GHz	16 dB	-20 dB	-14.4 dBm	0.840 mm ²	—	0.313	0.25 μm
[4]	1.5 – 4 GHz	-3 dB	-16 dB	-10 dBm	—	6 mW	0.350	0.18 μm
[5]	0 – 10 GHz	—	—	—	0.57 mm ²	1.44 mW	0.313	0.18 μm

Table 2. Comparison of various active CMOS baluns

highest found in the comparative circuits.

4. CONCLUSION

In this paper a compensating capacitor was introduced into the single transistor balun circuit to counter the effects of the parasitic capacitances C_{gs} and C_{gd} . A theoretical model was presented and verified through circuit simulations to demonstrate the effectiveness of the compensating capacitor. A common gate amplifier was placed at the input to improve the return loss and improve the gain. The measured results show that this new balun has a 7.5 GHz bandwidth, 15 dB return loss, -5.8 dBm compression point and 12 mW power consumption. These parameters when compared to existing devices prove to be very competitive, improving or equalling most devices in its class.

5. REFERENCES

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