Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Dominican Republic, Nov.3-5, 2004

# A Voltage-Variable Time Delay Element for Random Bit Waveforms

Yang Zhang and Carlos E. Saavedra

Department of Electrical and Computer Engineering, Queen's University

Kingston, ON Canada K7L 3Z6

***Abstract* - In this work, a concept for a voltage-variable time-delay circuit element for use with low data-rate random bit waveforms is demonstrated. The circuit operates by generating pulses at every rising and falling edge of the incoming bit stream. The pulses are elongated in time by an arbitrary amount using monostable multivibrators whose RC time-constant can be controlled by an applied voltage. The outputs of the multivibrators are used to trigger a pair of flip-flops and the delayed waveform is taken at the output of an exclusive-OR gate. Experimental results show that using this mechanism, the input signal can be delayed by up to 83 % of the signal period.**

## I. INTRODUCTION

Voltage-variable time delay circuits find wide use in communications devices for such applications as clock-recovery delay-locked loops (DLL's) [1-2]. Clock recovery circuits are one of the fundamental components of data transceivers, where they are used to synchronize the clock of the receiver with that of the transmitter device. Other important applications of variable time delay circuits include tapped delay-line filters.

A variety of delay elements have been proposed in previous works [3-6]. One of the most well known realizations uses cascaded inverters. These conventional delay circuits are attractive for their simplicity. With that approach, however, in order to obtain time delays approaching one clock period, several unit delay elements have to be cascaded, making the circuit large. This problem is aggravated if the bit data rate is low because the time delay obtained by a single inverter may be a very small fraction of the clock period.

In this paper, a new concept for a time-delay circuit is demonstrated that is especially suited for low data-rate applications (<< 1 Mbps). The proposed voltage-variable delay element has the advantage of being able to produce a variable delay of up to 83 % of the signal period. Therefore, this circuit has the potential to save significant amounts of silicon space. The delay element relies on a monostable-multivibrator (MS-MV) to generate wide duration pulses. The width of the pulses are controlled electronically by using a variable resistor implemented with a PMOS device.

The remainder of this paper is organized as follows: in Section II the operation of the circuit is discussed. In Section III the experimental results will be presented, and Section IV will conclude the work.

## II. CIRCUIT OPERATION

A block diagram of the proposed delay element is shown in Fig. 1, and Fig. 2 depicts sample waveforms at different points in the circuit. In this time delay circuit, the input signal first enters a transition detector, which generates two separate streams (A1 and B1) of short-duration pulses at the high-to-low and low-to-high transitions, respectively. The pulses in one stream indicate the time positions of every rising edge and in the other stream every falling edge in the data stream. The pulse streams subsequently enter a pair of monostable-multivibrators, or timers, which elongate the pulses in time by an arbitrary amount determined by a voltage variable resistor implemented using a PMOS transistor and a timing capacitor.

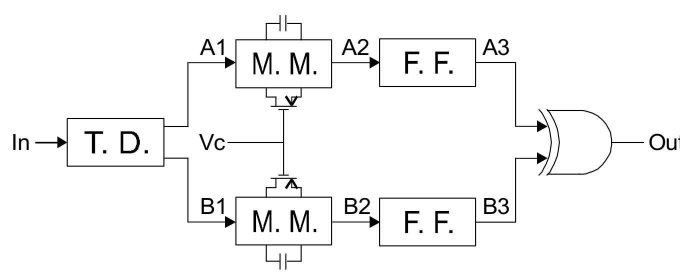


Fig. 1. Block diagram of the circuit.

The gates of the PMOS transistors associated with each timer are connected together in order to obtain the same pulse duration for the two pulse streams (A2 and B2). Next, the pulses are fed to a pair of negative edge-triggered flip-flops which toggle at the falling edge of every pulse. The outputs of the flip flops (A3 and B3) are combined using an exclusive-OR (XOR) gate and the result is a time-delayed version of the original bit stream. Thus, to change the delay, the value of the RC time constant in each monostable multivibrator must be changed by the same amount.

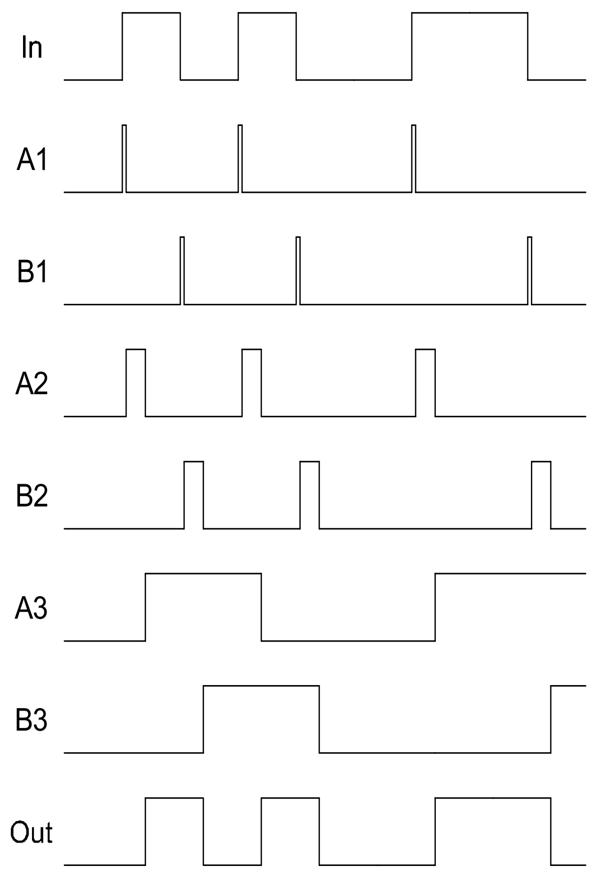


Fig. 2. Waveforms in each node of the circuit.

### A. Transition detector

The function of the transition detector is to find the temporal position of each low-to-high and high-to-low transition in the data stream. To detect an edge, whether rising or falling, the concept is to produce a replica of the same signal delayed by a short amount of time using an RC phase shifter. By feeding the input signal and an inverted time-shifted version of it (using an RC network) to a NAND gate, a pulse is generated at each low-to-high transition. A similar approach is used to generate the pulses at the high-to-low transitions (Fig. 3). The pulse width should be chosen as short as possible in order to increase the operating frequency. On the other hand, the pulses also have to be long enough so that the monostable multivibrator can detect them. In this work, the pulse width was chosen to be approximately 0.6 % percent of the clock period.

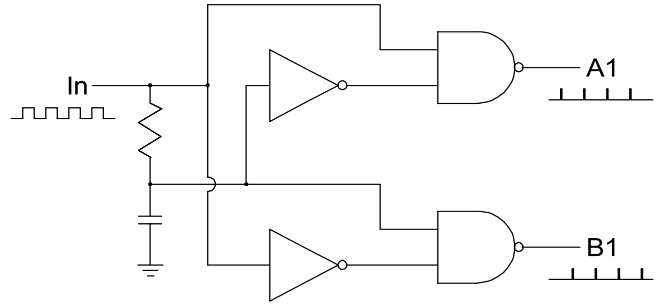


Fig. 3 Diagram of the transition detector.

### B. Monostable multivibrator

In order to generate a variable pulse signal, a potentiometer and a capacitor connected together with a monostable timer is commonly employed as an RC monostable multivibrator as depicted in Fig. 4. The pulse width is determined by the charge-up time of the capacitor. In this work, it is necessary to obtain two monostable pulses with the same time duration, and to this end, two multivibrators are used with the potentiometers replaced by a pair of identical PMOS transistors. The drain-source resistance of a P-channel MOSFET and the capacitor constitute the RC network. Thus, by applying the same gate-to-source voltage for the two PMOS devices, identical pulse widths were obtained.

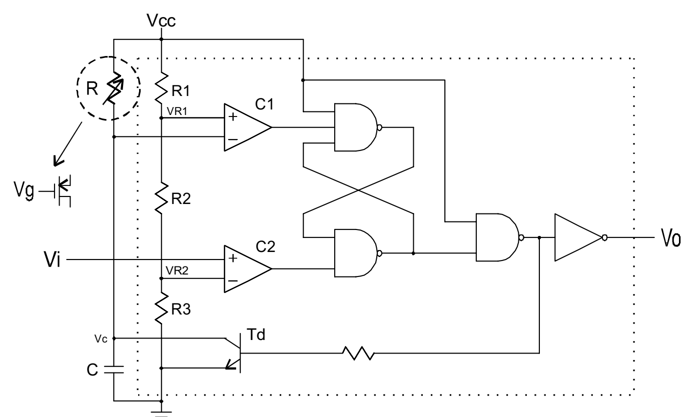


Fig. 4. A universal monostable multivibrator.

The resistance across the source and drain of the P-channel MOSFET, along with the capacitor C provides a path for current to flow from the power supply to ground, as shown in the portion to the left of the dotted box in Fig. 4. When a rising edge arrives at $V_i$, the output of the multivibrator rises to a high logic state and the transistor $T_d$ turns off. As a result, charge builds up across the capacitor C, which increases the voltage $V_C$. Once the voltage $V_C$ exceeds the positive node of the comparator $C_1$, $T_d$ turns on and the charge flows to ground through the transistor. When $V_C$ drops back to 0 V, the output falls down to logic level 0. Therefore, the pulse width is determined by the charging time of the capacitor through the

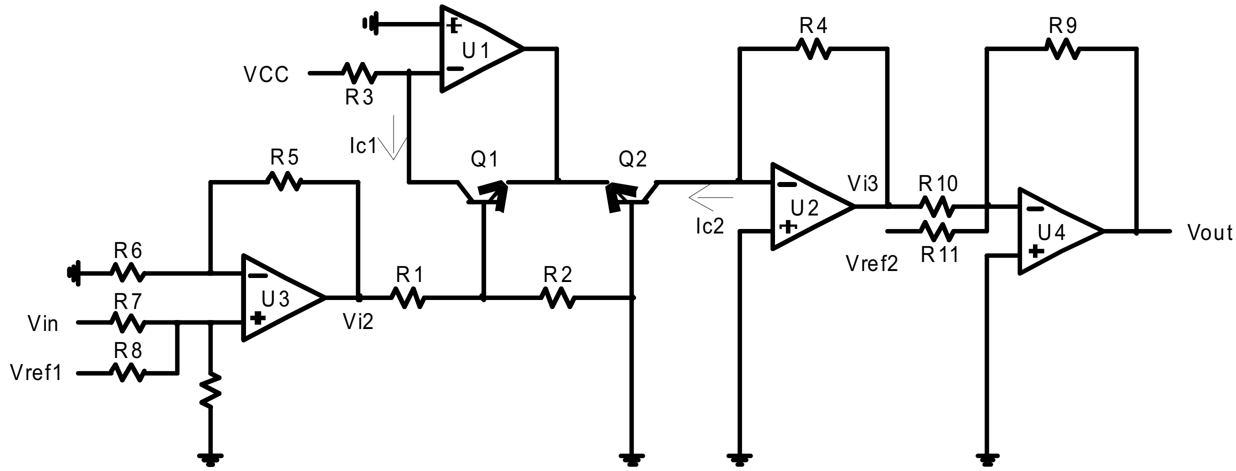


Fig. 6. Diagram of the compensation circuit.

PMOS resistor. One can change the charge-up time and hence the pulse width by varying the gate voltage of the transistor.

Because the value of the timing capacitor is small (the reason is explained in the next section), the transistor should be operated in its saturation region to achieve a large enough resistance to generate the monostable pulse with a width that is a significant fraction of the clock period. Writing a current node equation at the capacitor node and rearranging,

$$C\frac{dV_c}{dt} = \frac{1}{2}K_n(V_{GS} - V_{TH})^2 \qquad (1)$$

$$\frac{dV_c}{dt} = \frac{K_n(V_{GS} - V_{TH})^2}{2C} \qquad (2)$$

Since $R_1$, $R_2$ and $R_3$ are identical resistors in Fig. 4, the voltage across capacitor C is from 0 to 3.33V ($V_{CC}$ = 5V). Solving differential equation (2) above yields,

$$t = \frac{6.66C}{K_n(V_{GS} - V_{TH})^2} = \frac{6.66C}{K_n(V_G - V_{cc} - V_{TH})^2} \qquad (3)$$

Applying the transistor constant $K_n$ = 0.073 A/V$^2$, for this particular technology, the source voltage $V_{CC}$ = 5V, and threshold voltage $V_{TH}$ = -2.945V to equation (3), it is possible to calculate the final delay time of the bit stream as a function of the control voltage, $V_G$. Their characteristic curve is plotted as Fig. 5.

### C. Compensation Circuit

The curve plotted in Fig. 5 shows a highly non-linear relationship between the time delay and $V_G$. To moderate this dependence between the delay and applied voltage, a compensation circuit was designed. The concept is to pass $V_G$ through a non-linear circuit whose transfer function balances to a certain extent the one shown in Fig. 5. In effect, the applied gate voltage is "pre-distorted" in order to obtain a more linear delay-versus-control voltage relationship.

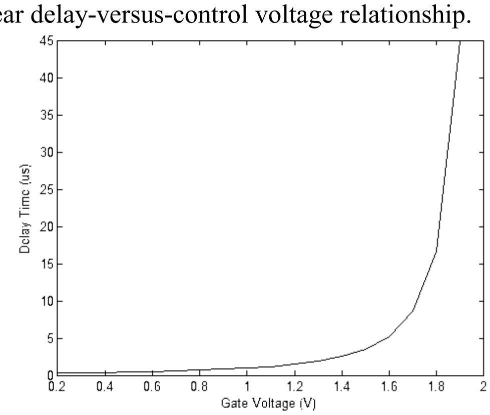


Fig. 5. Gate voltage versus delay time.

The compensation circuit (Fig. 6) consists four operational amplifiers and two bipolar devices. Amplifiers $U_1$ and $U_2$ in conjunction with transistors $Q_1$ and $Q_2$ yield an exponential voltage relationship. Amplifiers $U_3$ and $U_4$ are each connected as summing junctions, and their purpose is to allow for control of the vertical and horizontal axis location of the transfer function relating $V_{out}$ and $V_{in}$. To determine the relationship between $V_{out}$ and $V_{in}$, one begins with the current-voltage relationships of the bipolar transistors:

$$\frac{V_{BE1}}{V_t} = \ln\frac{I_{C1}}{I_s}, \ \frac{V_{BE2}}{V_t} = \ln\frac{I_{C2}}{I_s}$$

From which,

$$V_{BE2} - V_{BE1} = V_t \ln\frac{I_{C2}}{I_{C1}}$$

Then,

$$-\frac{R_2}{R_1+R_2}V_{i2}=V_t\ln\frac{I_{C2}}{I_{C1}}$$

The voltages $V_{i2}$ and $V_{i3}$ are related by,

$$-V_{i2}=(1+\frac{R_1}{R_2})V_t\ln\frac{V_{i3}R_3}{R_4V_{CC}} \quad (4)$$

And the output at the summing junction at $U_3$ is,

$$V_{i2}=\frac{R_5}{R_7}V_{in}+\frac{R_5}{R_8}V_{ref1} \quad (5)$$

Similarly, the output of $U_4$ is given by,

$$V_{out}=-\frac{R_9}{R_{10}}V_{i3}-\frac{R_9}{R_{11}}V_{ref2}\,. \quad (6)$$

Substituting (5) and (6) into (4) yields,

$$V_{out}=e^{\frac{-\frac{R_5}{R_7}V_{in}-\frac{R_5}{R_8}V_{ref1}}{(1+\frac{R_1}{R_2})V_t}}(-\frac{V_{CC}R_4R_9}{R_3R_{10}})-\frac{R_9}{R_{11}}V_{ref2} \quad (7)$$

Plotting equation (7) yields the graph in Fig. 7. From that expression it is straightforward to see the role played by the summing junctions at $U_3$ and $U_4$.

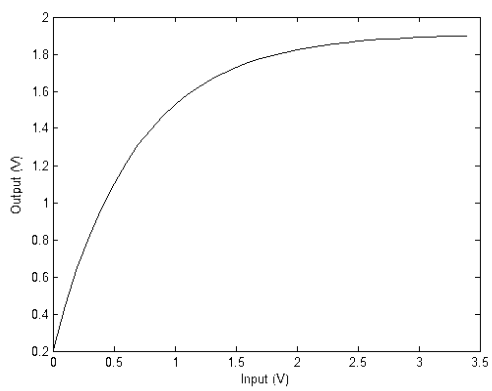


Fig. 7 Characteristics of the compensation circuit.

Substituting equation (7) into (3) with $V_{out}$ = $V_G$ and plotting the result in Fig. 8 reveals how the time delay-versus-control voltage relationship is improved by the compensation circuit.

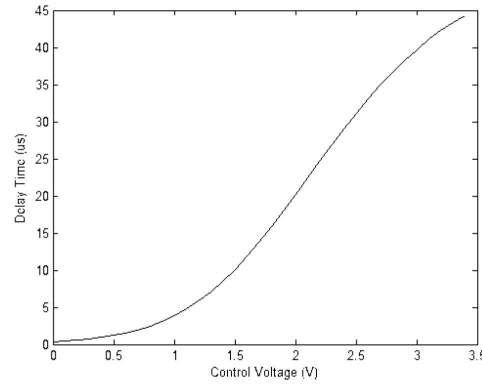


Fig. 8 Control voltage versus delay time in theory.

## III. EXPERIMENTAL RESULTS

Experimental time-domain voltage waveforms showing an input signal and a delayed version are shown in Fig. 9. The input signal is a periodic waveform with a period of 50 μs. Using a control voltage of 1.8 V, the time delay between the input and output waveforms is 15 μs. The system power supply voltage was 5.0 V. With this circuit, time delays between 0.5 μs and 41.5 μs were obtained. Thus, a continuous range of time delays between 1 % and 83 % of the clock period are possible with this circuit.

Fig. 10 shows experimental and theoretical curves for the time-delay versus applied control voltage with the compensation circuit. The agreement is very good, and the deviation between the two curves can be reduced by obtaining better device models.

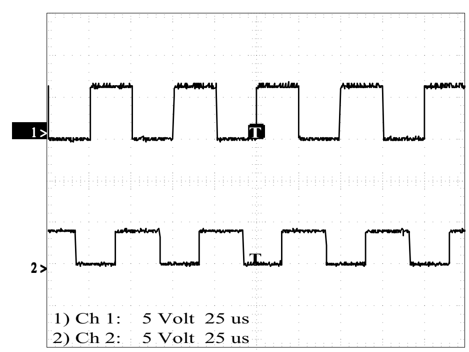


Fig. 9. Sample time-domain waveforms.

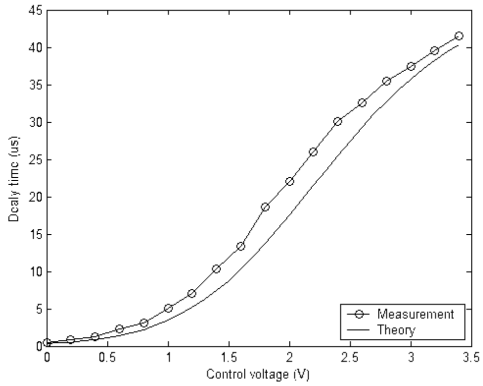


Fig. 10. Time delay versus control voltage using the compensation circuit.

When the control voltage applied to the delay circuit is 0 V, there is an "intrinsic" time-delay of about 0.5 μs at the output. This inherent time-delay comes from three sources. According to the waveforms in Fig. 2, it is seen that the small pulses generated by the transition detector are the first source of the inherent delay. Second, since the equivalent resistance between drain and source of the transistor in Fig. 4 will never be zero, it is not possible to achieve a zero time delay because it will take a certain amount of time for the capacitor to charge-up. Third, some amount of propagation delay in the logic gates after the multivibrator also contributes to the intrinsic delay. To reduce the intrinsic time-delay as much as possible, in addition to choosing high-speed logic gates, small capacitors should be used for the transition detector and the monostable multivibrator.

## IV. Conclusions

A time-delay circuit element for use with either periodic or random bit waveforms has been demonstrated. The circuit is capable of achieving long time delays of up to 83 % of the signal clock period. The core of the circuit consists of a pair of monostable multivibrators whose output pulse widths are controlled with voltage variable resistors implemented with P-channel MOSFETs.

## Reference


[1] H. Chang, J. Lin, C. Yang and S. Liu, "A Wide-Range Delay-Locked Loop with a Fixed Latency of One Clock Cycle," *IEEE Journal of Solid-State Circuits,* vol. 37, no. 8, August, 2002.

[2] R. Aguiar, D. Santos, "Multiple target clock distribution with arbitrary delay interconnects," *Electronics Letters,* vol. 34, no. 22, pp. 2119-2120, Oct. 1998.

[3] Mahapatra N. R., Tareen A., Garimella S. V., "Comparison and analysis of delay elements", *45th IEEE Midwest Symposium on Circuits and Systems*, Vol. 2, pp. 473-476, 2002.

[4] T. Lee, J. Bulzacchelli, "A 155-MHz clock recovery delay- and phase-locked loop," *IEEE Journal of Solid-State Circuits,* vol. 27, pp. 1736-1746, 1992.

[5] B. Garlepp, K. Donnelly, J. Kim, P. Chau, J. Zerbe , C. Huang, C. Tran, C. Portmann, D. Stark, Y. Chan, T. Lee and M. Horowitz, "A Portable Digital DLL for High-Speed CMOS Interface Circuits," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 5, May, 1999.

[6] G. Kim, M. Kim, B. Chang, W. Kim, "A Low-Voltage, Low-Power CMOS Delay Element," *IEEE Journal of Solid-State Circuits,* vol. 31, no. 7, July, 1996.

[7] Y. Zhang, C. E. Saavedra, "A Voltage-Variable time Delay Element for Clock Waveforms", *IEEE Canadian Conference on Electrical and Computer Engineering*, May 2004.